ISSN 2349-7815

International Journal of Recent Research in Electrical and Electronics Engineering (IJRREEE)
Vol. 4, Issue 4, pp: (1-7), Month: October - December 2017, Available at: www.paperpublications.org

A MATLAB Simulation Approach to Optimize the Electrical Characteristics of TFET & Estimation of Dynamic Resistance

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Abstract: **Tunneling field effect transistors (TFETs) have recently attracted considerable interest because of their potential use in low power logic applications. The major advantage of tunnel transistors is the possibility to achieve less than 60 mV/decade sub-threshold swing, which is the thermionic limit in conventional MOSFETs. Previously the tunnelling behaviour of the TFET is modelled by the reverse-biased Zener diode. This paper explored the cut in voltage and dynamic resistance of that Zener diode which helps to generate an effective MATLAB algorithm to facilitate efficient circuit design and simulation that well captures the electrical characteristics of the n-channel TFET.**

Keywords: **Tunneling field effect transistor, MATLAB algorithm, simulation, tunneling, dynamic resistance.**

1. INTRODUCTION

As the continuous down scaling of the conventional metal–oxide–semiconductor field-effect transistor (MOSFET) is approaching its fundamental limits, the need for a replacement device is growing. To overcome drawbacks like short-channel effects (SCE), and source-drain off-currents of the conventional MOSFET, a vertical field-effect transistor based on band-to-band tunneling has already been proposed [1], [2]. Also, for a conventional n-channel MOSFET, the input characteristics show exponential current increase only in the sub-threshold region, (gate voltage, V_G, is less then the threshold voltage, V_T). So far TFET is studied mostly experimentally or through device numerical simulation employing technology computer- aided design (TCAD). However, to facilitate the investigation of TFET-based circuits, a compact high-level SPICE model with moderate accuracy needs to be developed. Conventionally, there are two ways of device modeling for circuit simulation, i.e., one based on the analytical expressions generally extended from simplified device physics and the other based on a table lookup. Although the analytical-based modeling [3] provides insight to the device operation and limitations, it is often difficult to develop at an early stage for newly proposed devices due to a lack of in-depth understanding of the device physics. In addition, the analytically derived model could easily end up with numerous fitting parameters, which require sophisticated global optimization program development, and long computational time to achieve a reasonable agreement with the measured device characteristics. On the other hand, although table lookup modeling provides an easy and straight forward method to model new devices based on the measured or simulated (TCAD) device characteristics [4]–[5], it is not easily scalable, and the incorporation of the table lookup model could be both time consuming and complicated.

In this brief, we propose a semi empirical high-level SPICE behavioral model for the TFET device. It makes use of a Zener diode to model the tunneling behavior of the transistor with the addition of dependent sources to incorporate the device's current dependence on terminal voltages.

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2. DEVICE PHYSICS

Inter-band tunneling was first observed in 1957 by Esaki [7] while studying narrow forward-biased p–n junctions called tunnel diode. This device has been used in LP microwave applications such as local oscillators for communication and high-speed sampling. A reverse-biased tunnel diode (Zener diode) can be used as a transistor by using a gate contact to control the band bending in the channel region [8].

The device consists of a three terminal gated p-i-n diode with a heavily doped 3-nm p layer at the p-source end as shown in Fig. 1. This heavily doped p layer leads to the pinning of the Fermi level at source end. Applying a positive gate voltage, V_{GS} , results in a n-inversion channel at the oxide-silicon interface. This causes the formation of a sharp p n tunnel junction between the heavily doped p-source and the inverted channel. Thus, the gate directly controls the p^+n^- junction width which we define as the tunnel barrier width, Applying a drain voltage, V_{DS} , pulls the bands further down, thereby lowering . However, this happens only for low as the tunnel widths soon saturate. The device input characteristics are determined by Zener tunneling of a gate-controlled reverse biased p n junction. The output characteristics initially show an exponential behavior (for low V_{DS}) and then perfect saturation. The working principle and performance of the device has been discussed in detail by means of both experimental and simulation results [4], [5], [6].

Fig. 2 illustrates the energy band diagrams of an N-TFET under different bias conditions. At zero bias, majority carriers in both the channel and the drain see huge potential barriers, as shown in Fig. 2(a), and the drain current is due to reverse-biased leakage current in a p-i-n structure. When a positive gate bias is applied, the energy band at the channel region bends downward, leading to the formation of an inversion layer of electrons, which extends from the n-type drain to the p-type source, as illustrated in Fig. 2(b). An additional positive drain bias shifts down the Fermi levels in both the n-type drain and the inversion layer channel. If the downshift is large enough to narrow the tunneling width formed by the conduction band and the valence band at the source–channel junction, a tunneling path will be formed, allowing electrons to tunnel from the source to the channel, as shown in Fig. 2(c). It is the gate modulation of the tunneling width that allows the TFET to achieve a lower subthreshold swing than the conventional MOSFET.

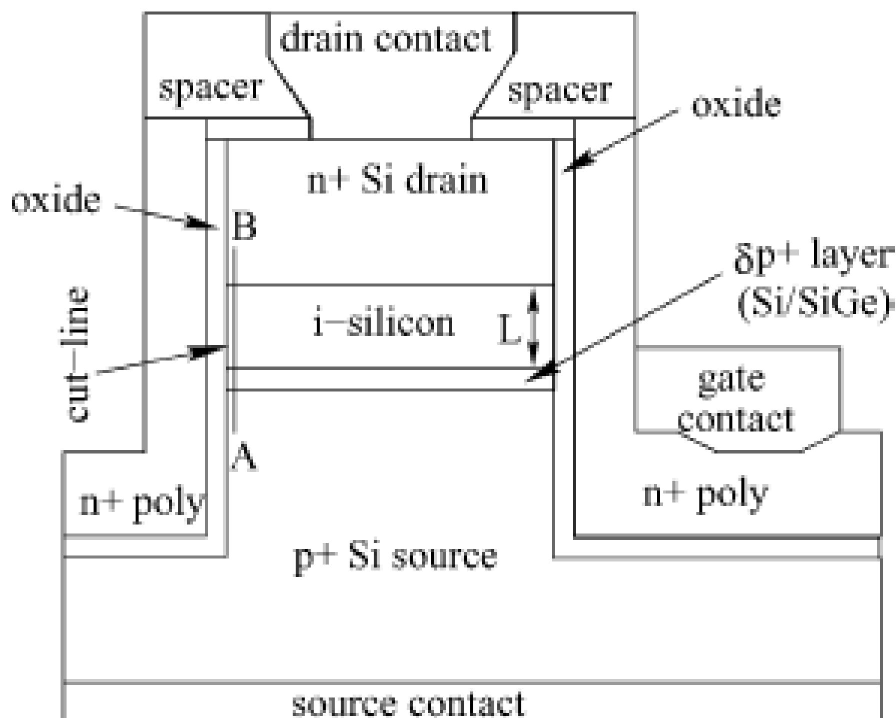

Fig 1: Schematic representation of the Esaki Tunnel FET structure. A-B represents the cut-line, close to and parallel to the Si-SiO_2 interface for the band-diagrams

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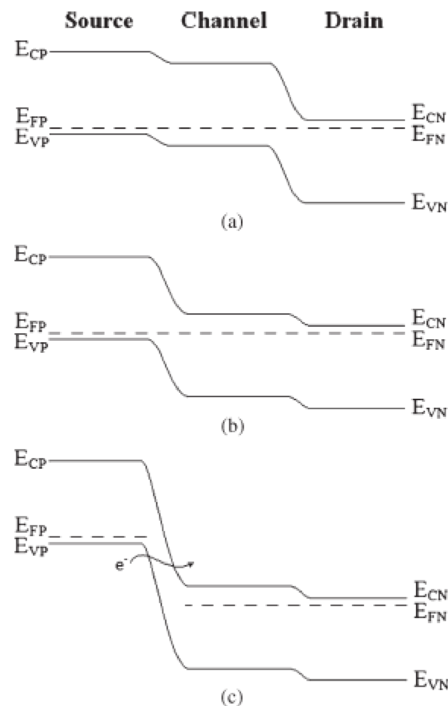

Fig 2: Simplified energy band diagram of an N-TFET at (a) Vgs = Vds = 0, b) Vgs > 0 and Vds = 0, and (c) Vgs > 0 and Vds > 0.

3. TUNELLING BEHAVIOUR AND MODELLING WITH ZENER DIODE

The device physics of tunnel field effect transistor suggests that it may be modeled using a Zener diode. Because Zener diode also exhibits the tunneling behavior under reverse bias. Direct tunneling can occur between two extrema, located at the same point in K space. The "forbidden' gap is bridged by proceeding along the imaginary K axis. This idea has been previously explored by T.Niroschi.et.al (9). But this primitive model was further corrected for CMOS in his next work (10). It only models the dependence of the electrical. characteristics on the drain to source voltage. As mentioned earlier the gate to source voltage also helps the band bending at the source channel junction and contributes to the tunneling behavior. This phenomenon should be captured for accurate TFET modeling. The semi-empirical compact spice model is shown in figure 3.

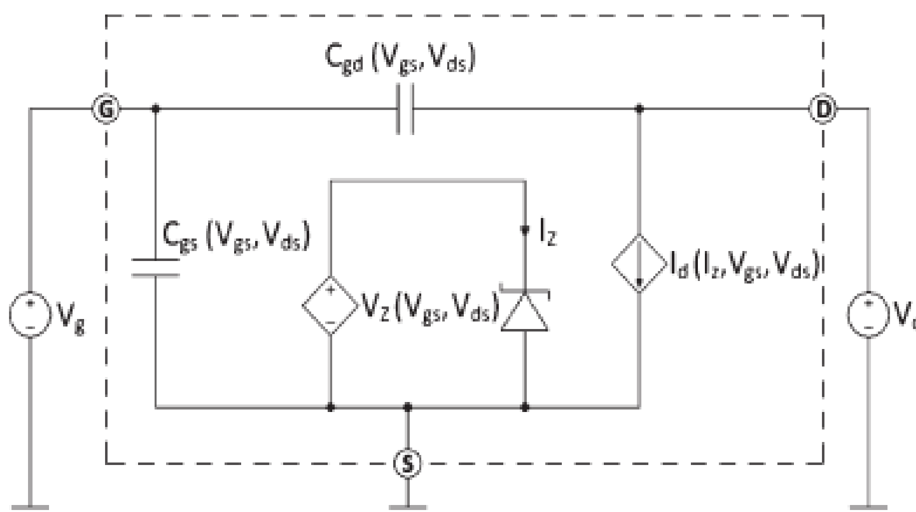

Fig 3: Spice TFET Model

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For that reason two levels are used to model the dependence of the current on terminal voltage .The first level is the reverse biased voltage V_z (V_{GS},V_{DS}) that effects the zener diode current (I_z). So Iz is a function of both V_{gs} and V_{ds} .Then in next level drain current Id is modeled as a dependant current source as a function of tunneling current I_z, gate to source voltage Vgs and drain to source voltage Vds .In this work cut in voltage and dynamic resistance of the zener diode is explored which helps to formulate the mathematical expression which clearly depicts the dependence of I_z on V_z which in turn depends on V_{gs} and V_{ds}. This paper uses some relevant parameters which is extracted by employing the 2-D TCAD Tool General Purpose Semiconductor Simulator (GSS) (11,12). Table 1 shows the summary of Parameter Values extracted using GSS. It is nontrivial to obtain the corresponding V_Z and I_D. The V_Z –V_{GS} relationship at different Vds's is first

TABLE I: SUMMARY OF PARAMETER VALUES FOR V_Z AND I_d

Parameter	Value	Parameter	Value
A	0.200	K	0.300
B	0.220	L	0.600
C	0.100	M	0.050
D	1.000	N	4×10^{-11}
E	3.800	O	0.280
F	5.974	P	0.001
G	0.473	Q	2.500
H	0.400	R	0.125
I	0.300	S	1.000
J	6.030	T	0.800

Obtained by mapping the desired I_D. This allows us to determine the empirical functions defining the V_Z based on mathematical knowledge on behaviour. In spite of the available information about reverse Zener voltage, it is insufficient to construct a MATLAB algorithm. Because, the functional dependence between Vz and Iz is still required. In order to find out Zener current-voltage relationship of the zener diode specified in spice model suitable optimization technique is employed for different drain source voltages. It provides excellent matching with the values of drain current for different gate source voltage keeping drain to source voltage constant. Simultaneously the Zener voltage is determined using empirical mathematical relationship. The relationship between projected zener current and voltage is shown in figure 4

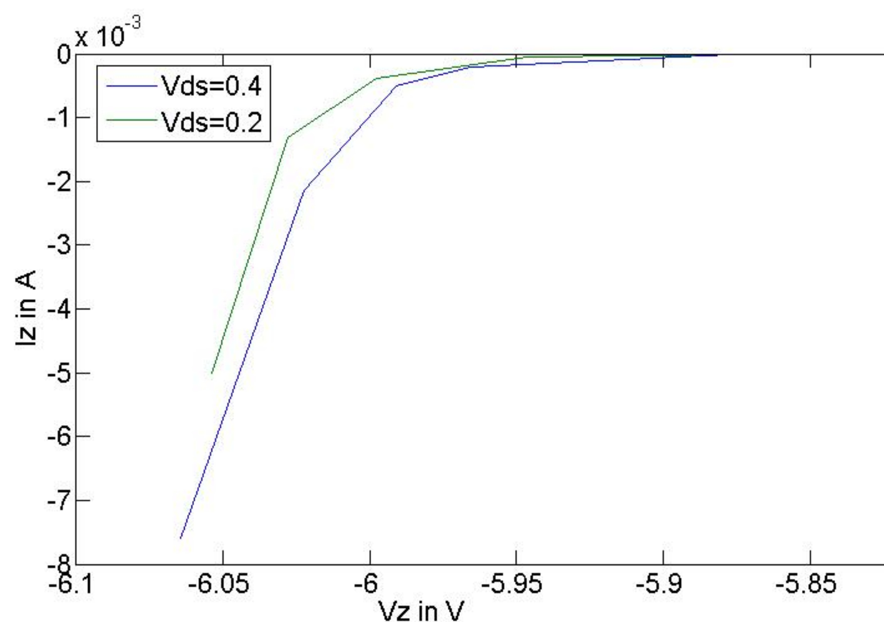

Fig 4: Characteristics of Zener diode specified in SPICE model

ISSN 2349-7815

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After suitable 4th order polynomial curve fitting shown in figure 5 the mathematical dependence function between Vz and Iz is formulated.

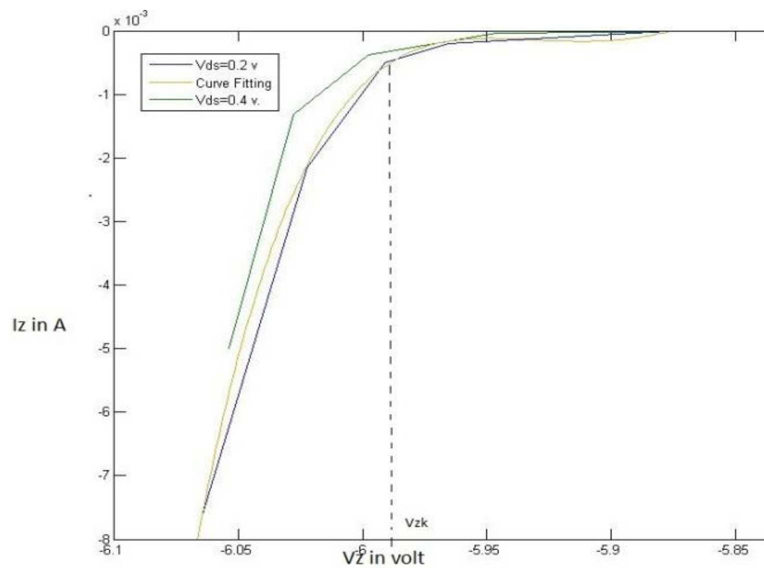

Fig 5: Dependence of Iz on Vz captured by 4th order polynomial Curve Fitting Method

4. PROPOSED MATLAB ALGORITHM

In this study a MATLAB algorithm is proposed to find out the electrical characteristics of tunneling field effect transistor. This algorithm gives excellent result for the TFET with p type source and n type drain. The doping concentration of p type source and n type drain are taken as 10^{20} cm^{-3} and 10^{19} cm^{-3} respectively. The channel is lightly doped p type semiconductor with a concentration of 5×10^{16} cm^{-3}. The algorithm is described in following section

Step 1:-

The VGS & VDS values are taken from the user as input.

Step 2 :-

The V_{DS} is compared with (V_{GS}-C) & if the result is greater than VDS then VDS1 is equal to V_{DS} else V_{DS1} is equal to V_{GS}-C.

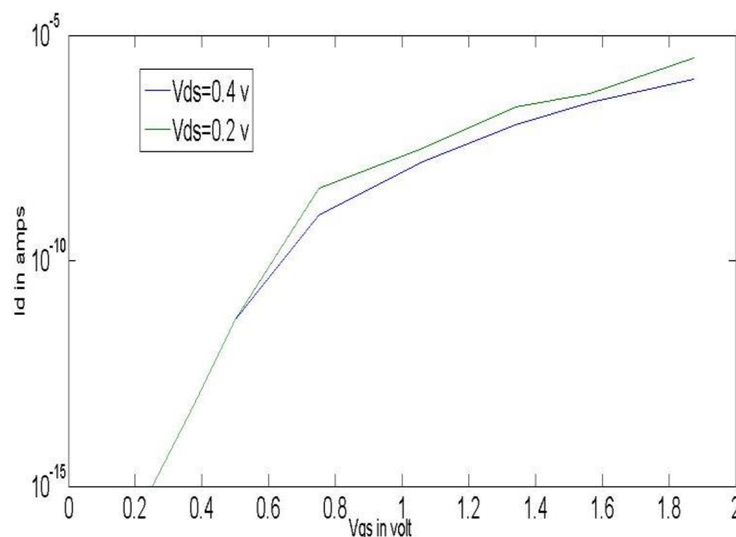

Fig 6: MATLAB Simulated Vgs vs Id plot

Step 3:-

Now, if VDS1 is greater than equal to L Vz2 is equal to

$Iln(Vgs - C) + J$ else

Vz2 = $Iln(Vgs - C) + J - K(L - Vds1)^2$.

Step 4:-

If V_{DS1} is greater than equal to H, then $V_{Z1}$is equal to $Bln(Vgs - C) - \frac{1}{2}\left(\frac{Vgs-D}{E}\right)^2 + F$ else V_{Z1} is equal to $Bln(Vgs - C) - \frac{1}{2}\left(\frac{Vgs-D}{E}\right)^2 + F - G(H - Vds')^2$.

Step 5:-

If VGS is greater than equal to A ,V_Z will be the minimum of V_{Z1} and V_{Z2} else V_Z is equal to five.

Step 6:-

If V_{DS1} is greater than equal to T, then f_3 is equal to one else zero.

Step 7:-

If V_{GS} is greater than equal to V_{DS1} , then f_2 is equal to $(V_{GS}-V_{DS1})^2$ else f_2=0.

Step 8:-

If V_{GS} greater than equal to T ,then f_1 will be equal to $(V_{GS}-T)^2$ else f_1=0.

Step 9:-

If Vz is less than Vzk , Iz=0 else $Iz=10Vz^4-2.3\times10^2\ Vz^3+ 2.1\times10^3\ Vz^2 -8.1\times10^3 Vz +1.2\times10^4$.

Step 10:-

We calculate Id3 which is given by

$$Id3 = PIze^{\left(\frac{f1-f2}{Q}\right)}e^{\left(-f3\frac{f1-f2}{R}\right)}[1 + S(Vds1 - T) .$$

Step 11:-

If V_{DS} is greater than V_{DS1}, then Id2 equals to $Id3\big(1 + O(Vds - Vds1)\big)$, else if V_{DS} is equal to V_{DS1} then Id2=Id3 else we move on to the next conditional statement.

Step 12:-

We calculate Id_1 where Id1= NV_{DS1}. If V_{DS1} is less than M , Id will be the minimum amongst Id1 and Id2 else Id=Id2

5. RESULTS & DISCUSSION

Gate to source voltages and drain to source voltages in form of two different arrays can be given as input. To, obtain V_{GS} vs Id plot the data of V_{DS} array is kept constant. The simulated result is shown in figure 5.

Table 2(a): Comparison with SPICE for VDS=0.2V

V_{GS} in Volt	Id from PSPICE (in A)	Id from MATLAB (in A)	Percentage error
0.5	5.01×10^{-12}	5.0123×10^{-12}	0.05%
0.75	10^{-9}	1.0278×10^{-9}	2.78%
1.062	1.585×10^{-8}	1.582×10^{-8}	0.19%
1.34	10^{-7}	1.0156×10^{-7}	1.56%
1.562	3.162×10^{-7}	3.161×10^{-7}	0.03%
1.875	10^{-6}	1.0337×10^{-6}	3.40%

Table 2(b): Comparison with SPICE for VDS=0.4V

V_{GS} in Volt	Id from PSPICE(in A)	Id from MATLAB (in A)	Percentage error
0.5	5.013×10^{-11}	5.012×10^{-11}	0.02%
0.75	7.94×10^{-9}	7.941×10^{-9}	0.01%
1.0625	10^{-7}	1.035×10^{-7}	3.50%
1.1875	2.51×10^{-7}	2.512×10^{-7}	0.08%
1.375	10^{-6}	1.0067×10^{-6}	0.67%
1.75	3.16×10^{-6}	3.16×10^{-6}	0.00%

The simulated V_{GS}-Id characteristics for constant V_{DS} clearly depicts that for $V_{DS} < 0.25$ volt drain current is very nominal and it almost remain constant. But as the gate to source voltage progresses drain current increases in a specific manner. In Table 2 simulated result using MATLAB is compared with the SPICE simulated result and it shows maximum 4% deviation. Also from the Zener characteristics shown in figure 4 the dynamic resistance is calculated, which is nearly 10 ohm irrespective of varied gate to source voltage.

6. CONCLUSION

A behavioral MATLAB algorithm of the Esaki Tunneling FET is developed to capture the I-V characteristics. The proposed algorithm has an accuracy of 4% in modeling I-V characteristics. So, this work allows us to perform MATLAB circuit simulation of TFET based circuit with moderate accuracy.

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